**ARM ISA**

* **Characteristics**
* RISC aspects
  + Instructions have fixed length (32 bits)
  + Only load/store instructions can access memory
  + Arithmetic/logic instructions only operate on registers
* CISC aspects
  + Auto-increment/-decrement and PC-relative addressing modes
  + Condition codes (N, Z, V, C) are used for conditional execution of instructions
  + Multiple registers can be loaded/stored from/to a block of memory
* Memory organization
  + Byte-addressable, 32-bit address space
  + Supports little/big-endian
  + Supports data sizes of words (32), half words (16), bytes (8)
* Registers
  + 16 32-bit registers R0 – R15
  + R15 = PC; R12 = frame pointer (by convention); R13 = stack pointer; R14 = link register
  + CPSR/PSR = status register – conditional code flags